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NORTH AMERICA 2025

Unlocking 15% More Performance: A Case Study in LLVM Optimization for RISC-V

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Unlocking ~~15%~~ 16% More Performance: A Case Study in LLVM Optimization for RISC-V

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Up to 16% faster SPEC CPU® 2017 on SpacemiT-X60

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- Our target board was the Banana Pi BPI-F3 with a SpacemiT-X60 8-core RISC-V processor:
  - In-order processor.
  - Supports the RVA22U64 Profile and 256-bit RVV 1.0 standard.

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- Our goal: to close the performance gap between LLVM and the GCC compiler.
- Our result: individual contributions boosted performance by up to 16% on SPEC CPU® 2017 benchmarks.

The Project

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- Prior to this work, a clear performance gap existed between code generated by LLVM and GCC for RISC-V.
- There is no single solution to close the gap, as improvements and regressions occur daily within the codebase.
- This presentation will focus on our three main contributions to help close the gap:
  - Introducing a scheduling model for the SpacemiT-X60.
  - Improvements to vectorization across calls.
  - Register Allocation with IPRA Support for RISC-V.

Our Contributions

(major contributions first)

SpacemiT-X60 Scheduling Model

SpacemiT-X60 Scheduling Model

- Instruction Scheduling == Performance.
- Wrong latencies/resources → compiler makes poor choices.

```
fld     ft0, 0(a0)
fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

before

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
fadd.d  ft1, ft0, ft2
```

after

SpacemiT-X60 Scheduling Model

- Instruction Scheduling == Performance.
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Load latency not modelled

```
fld     ft0, 0(a0)
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```

before

```
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fadd.d  ft1, ft0, ft2
```

after

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Dependent on ft0 → stalls

```
fld     ft0, 0(a0)
fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

before

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
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```

after

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```
fld     ft0, 0(a0)
fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

Issued later, independent

before

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
fadd.d  ft1, ft0, ft2
```

after

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```
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fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

before

Load issued

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
fadd.d  ft1, ft0, ft2
```

after

SpacemiT-X60 Scheduling Model

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```
fld     ft0, 0(a0)
fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

before

Independent op fills load latency

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
fadd.d  ft1, ft0, ft2
```

after

SpacemiT-X60 Scheduling Model

- Instruction Scheduling == Performance.
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```
fld     ft0, 0(a0)
fadd.d  ft1, ft0, ft2
fmul.d  ft3, ft4, ft5
```

before

Now executes with result ready

```
fld     ft0, 0(a0)
fmul.d  ft3, ft4, ft5
fadd.d  ft1, ft0, ft2
```

after

How We Got the Numbers

- We built custom microbenchmarks to measure instruction latencies.

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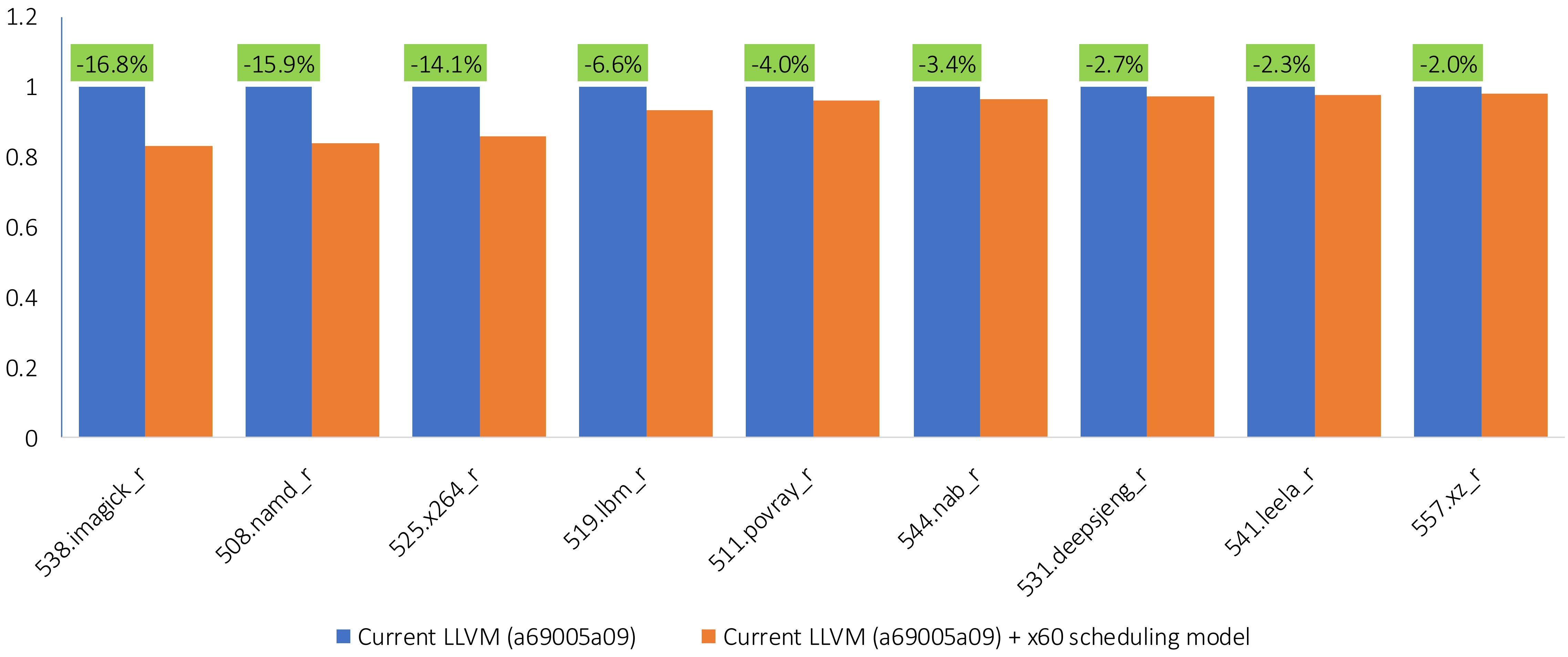
- We built custom microbenchmarks to measure instruction latencies.
- Most of instruction throughput data available at https://camel-cdr.github.io/rvv-bench-results/bpi_f3/index.html.
- It’s RISC but:
  - 201 scalar instructions.
  - 82 floating-point instructions.
  - 9185 RVV instructions (because of the combination of different LMULs and SEWs).

RVA22U64 SPEC exec time, O3+LTO+mcpu=spacemit-x60



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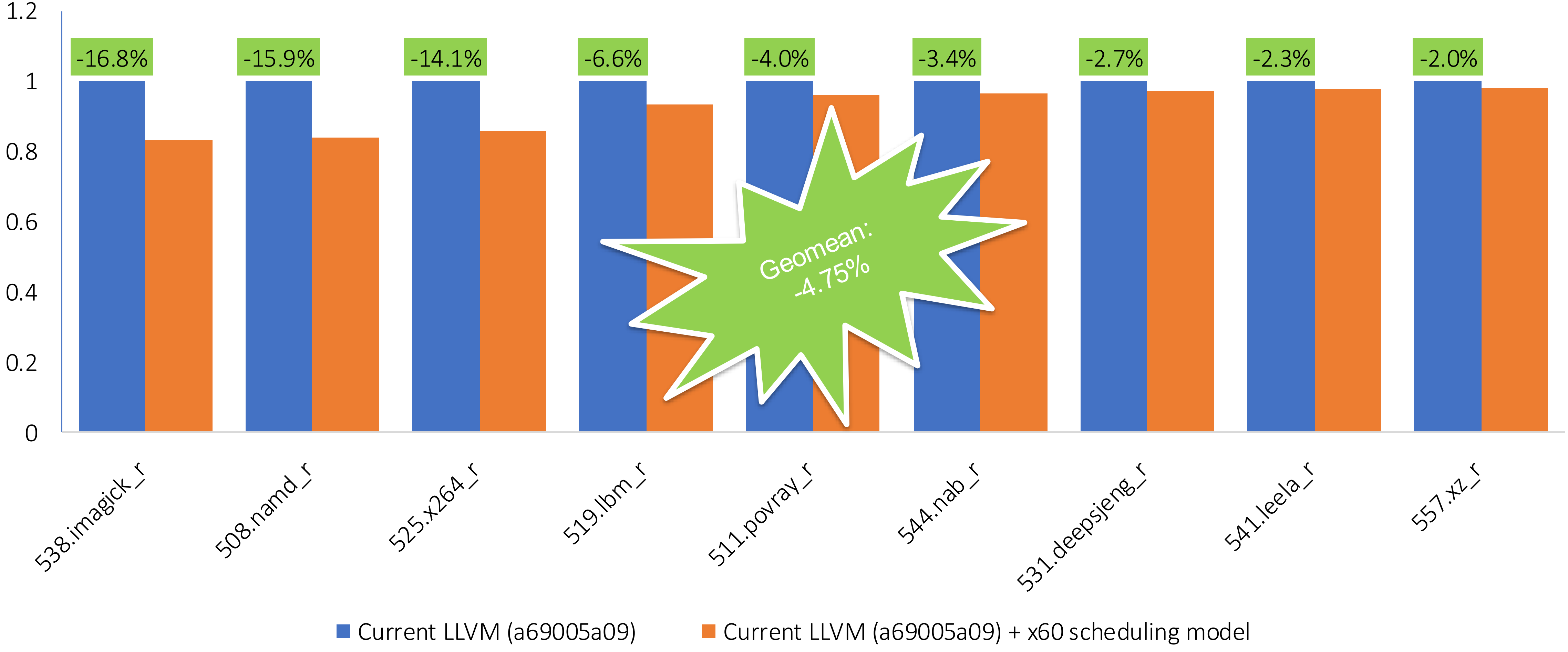
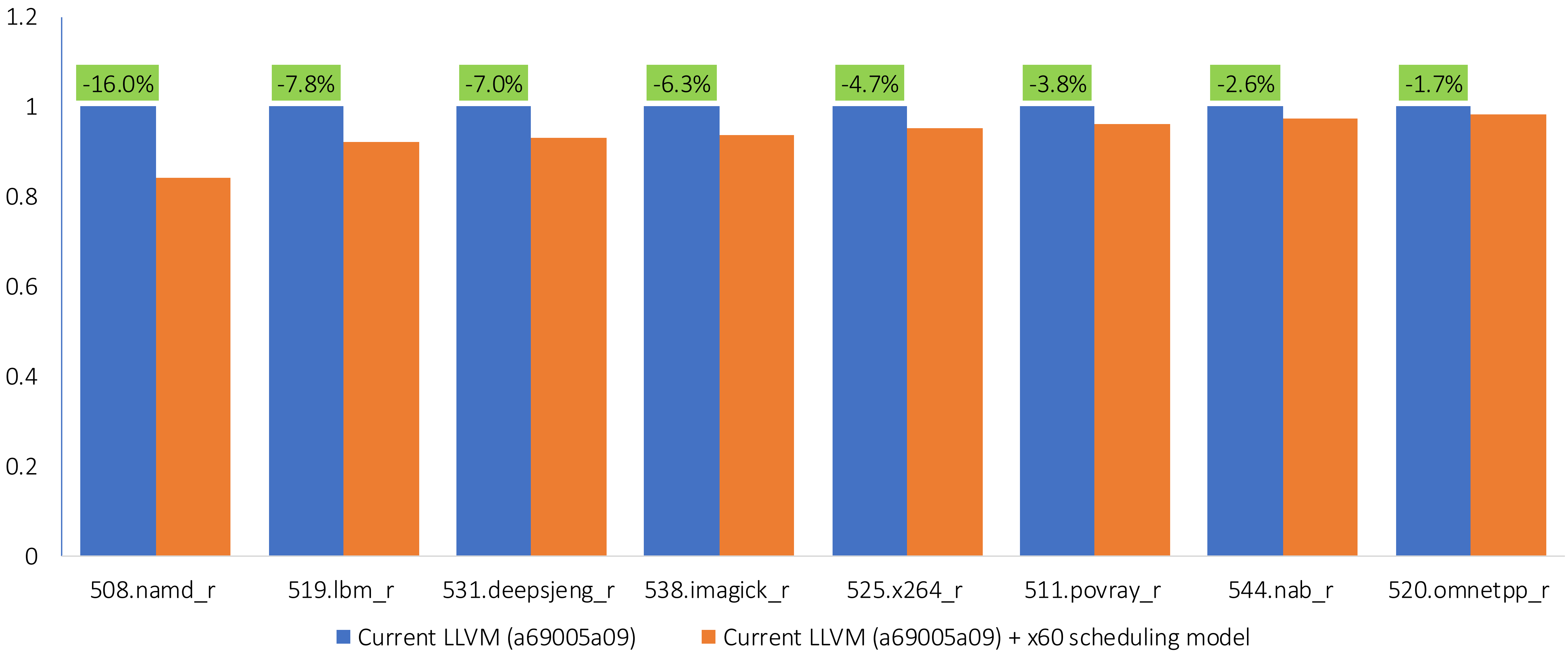
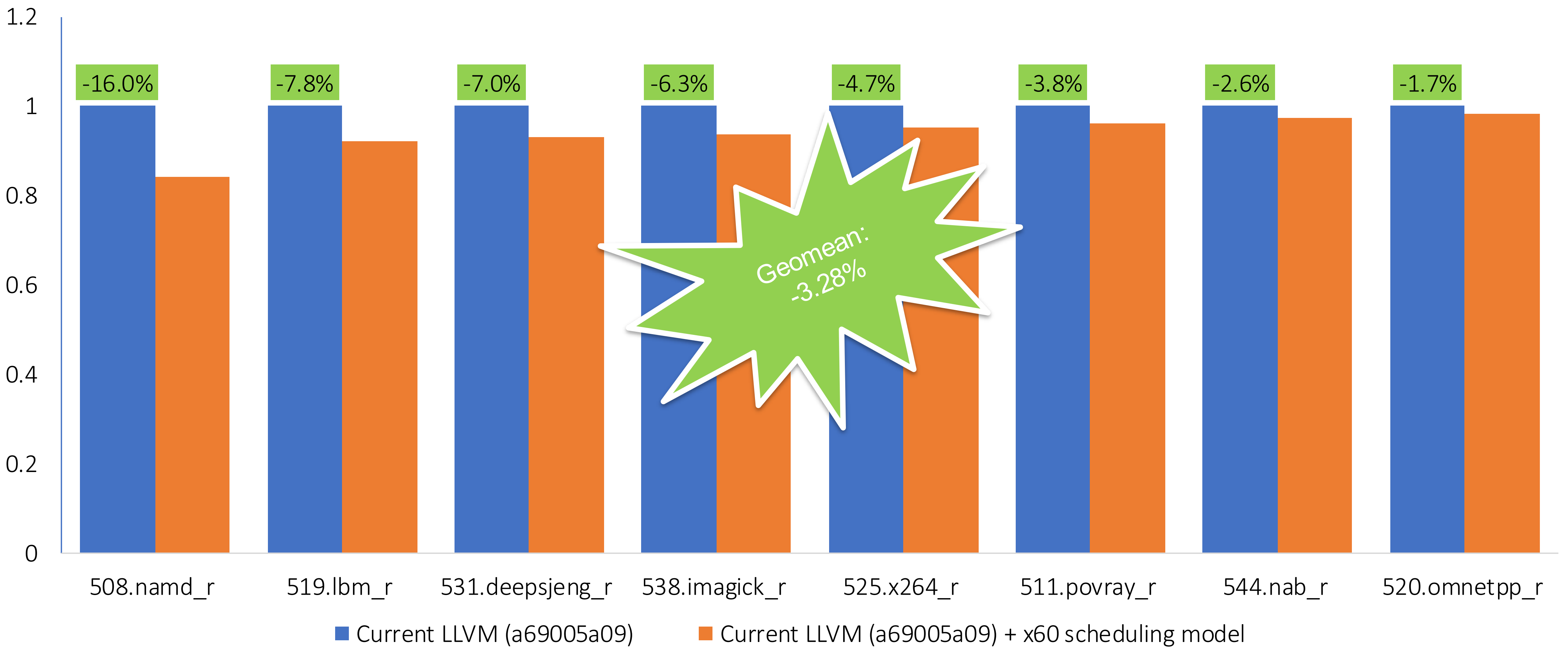


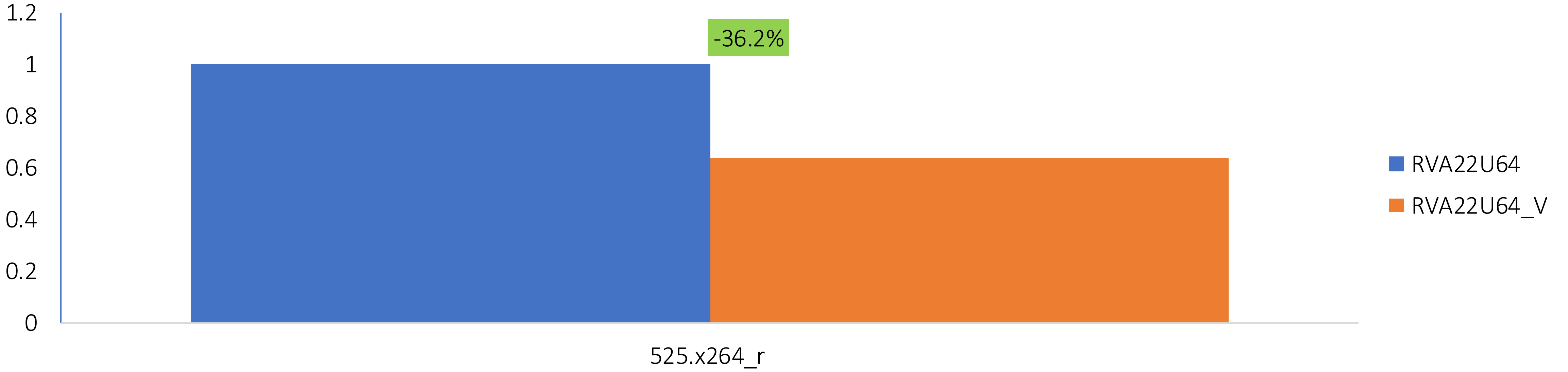
RVA22U64_V SPEC exec time, O3+LTO+mcpu=spacemit-x60



RVA22U64_V SPEC exec time, O3+LTO+mcpu=spacemit-x60

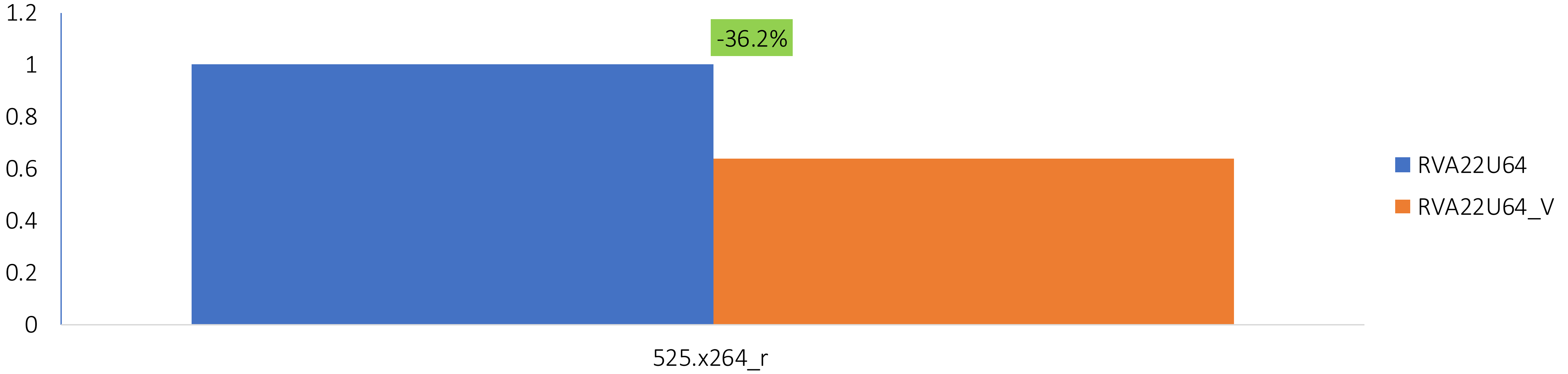


RVA22U64 vs RVA22U64_V, O3+LTO+mcpu=spacemit-x60



- Scheduling nearly eliminated the gap between scalar and vector configs.

RVA22U64 vs RVA22U64_V, O3+LTO+mcpu=spacemit-x60



- Scheduling nearly eliminated the gap between scalar and vector configs.
- On in-order processors like X60, scheduling is critical; on out-of-order, impact would be smaller and vectorization more decisive.

Improvements to Vectorization Across Calls

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- Root cause: poor cost modeling and suboptimal spill behavior.

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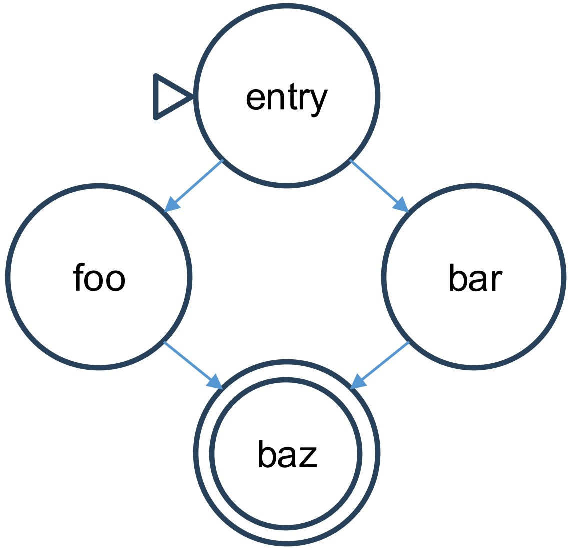
- Initial surprise: vectorized code sometimes underperformed scalar.
- Root cause: poor cost modeling and suboptimal spill behavior.
- The extra cycles were due to register spilling, particularly around function call boundaries.

The 544.nab_r case

```
define void @f(i1 %c, ptr %p, ptr %q) {
entry:
  %x0 = load i64, ptr %p
  %p1 = getelementptr i64, ptr %p, i64 1
  %x1 = load i64, ptr %p1
  br i1 %c, label %foo, label %bar
foo:
  call void @g()
  br label %baz
bar:
  call void @g()
  br label %baz
baz:
  store i64 %x0, ptr %q
  %q1 = getelementptr i64, ptr %q, i64 1
  store i64 %x1, ptr %q1
  ret void
}
```



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Loads first value from %p

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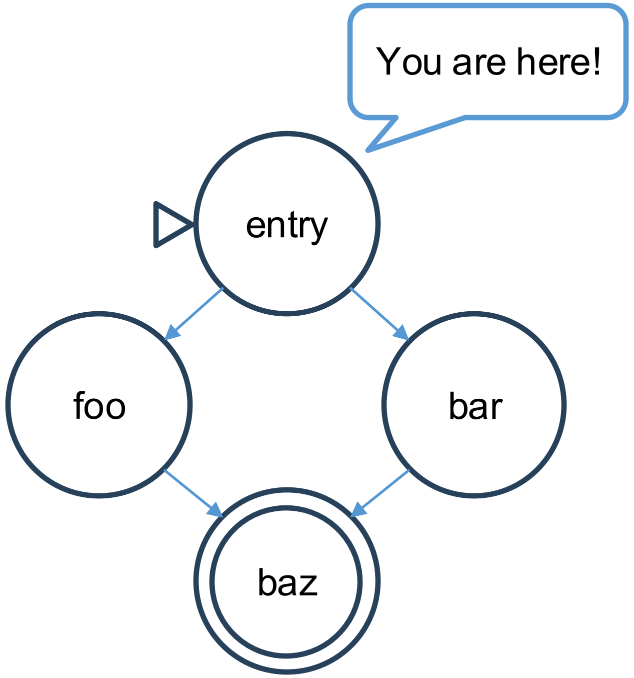

The 544.nab_r case

Loads second value from %p

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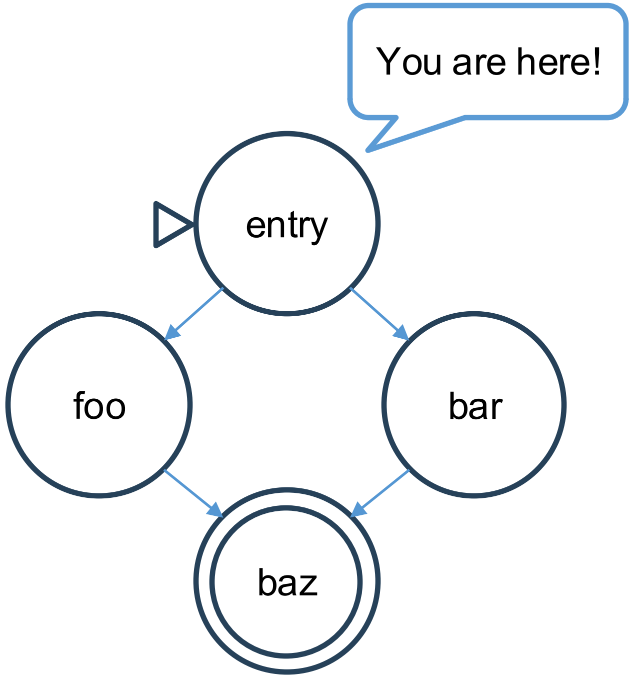

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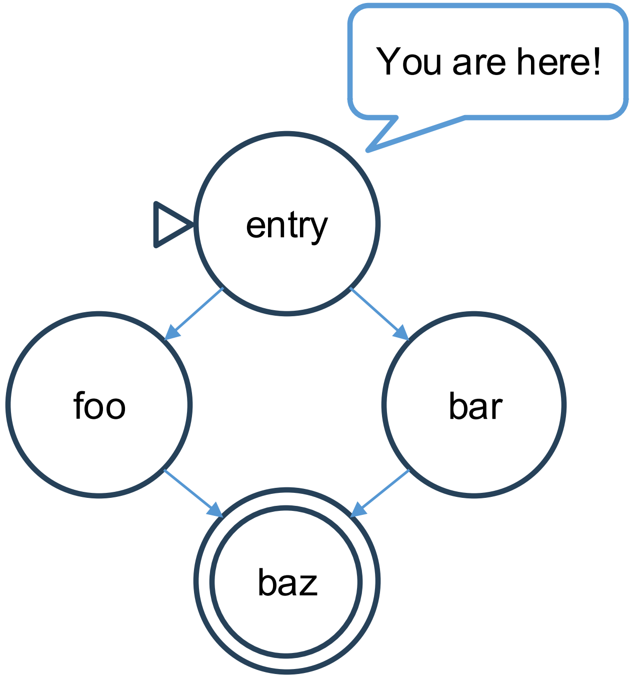
```

Conditional jump



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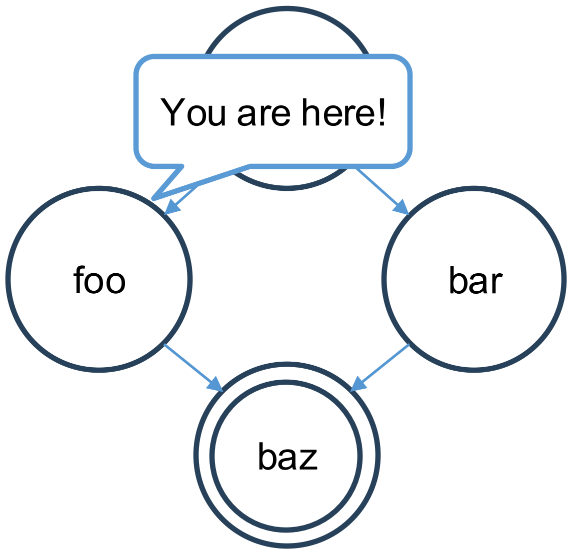
Conditional call to g()



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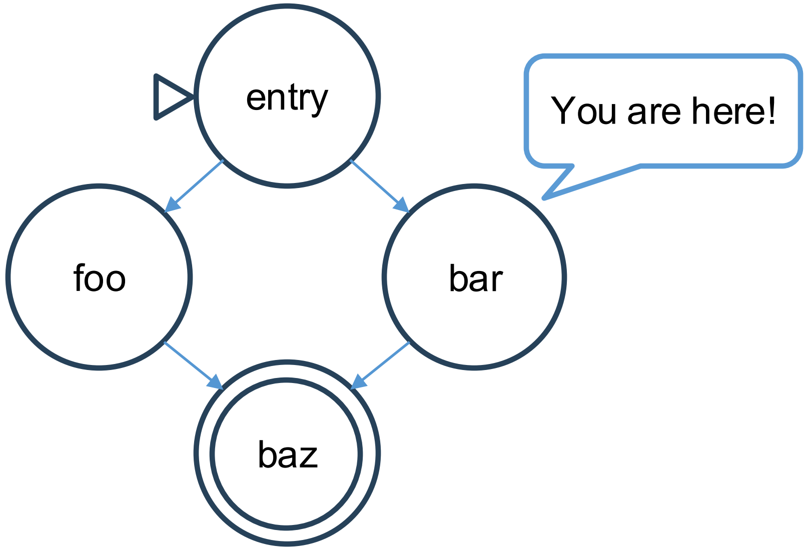

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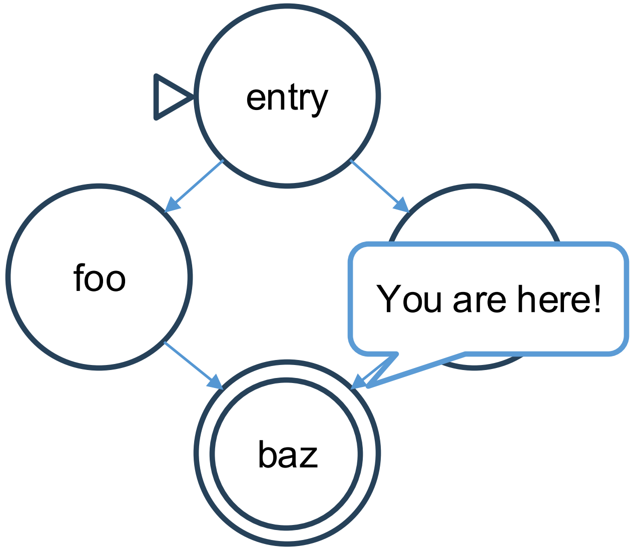
Stores first value from %q



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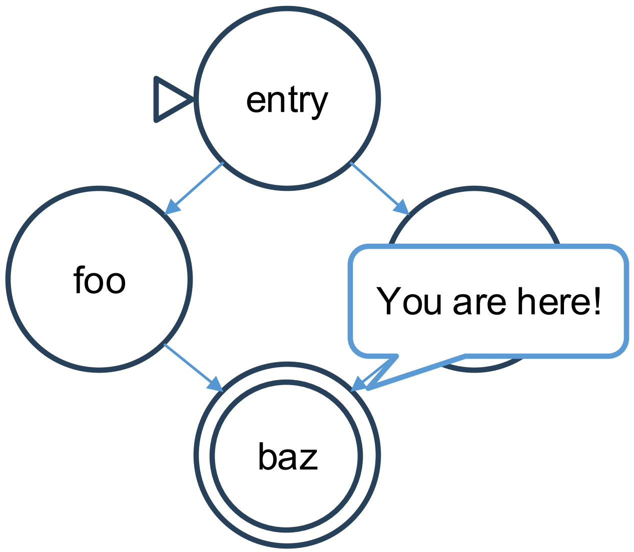

Fixing Real Bugs

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- Since we are storing and loading from continuous regions, the accesses can be vectorized.
- We found that the SLP Vectorizer was aggressively vectorizing regions without properly accounting for the cost of spilling vector registers across calls.
- Previously, the SLP vectorizer only analyzed the entry and baz blocks, ignoring foo and bar entirely.

The 544.nab_r case

Not being analyzed

```
define void @f(i1 %c, ptr %p, ptr %q) {
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  %x0 = load i64, ptr %p
  %p1 = getelementptr i64, ptr %p, i64 1
  %x1 = load i64, ptr %p1
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foo:
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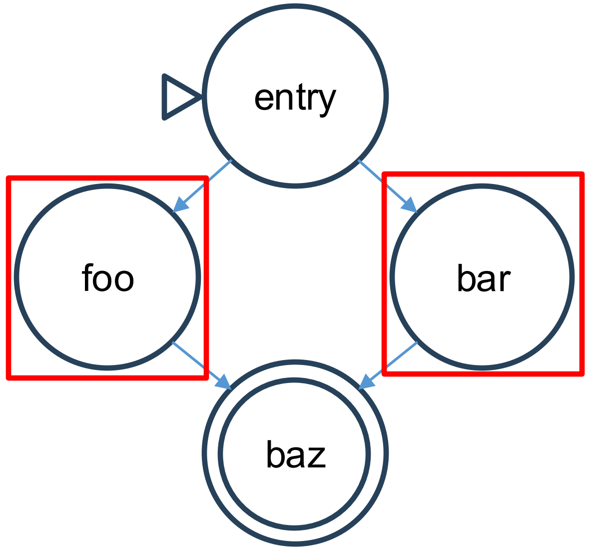

Addressing the Issue

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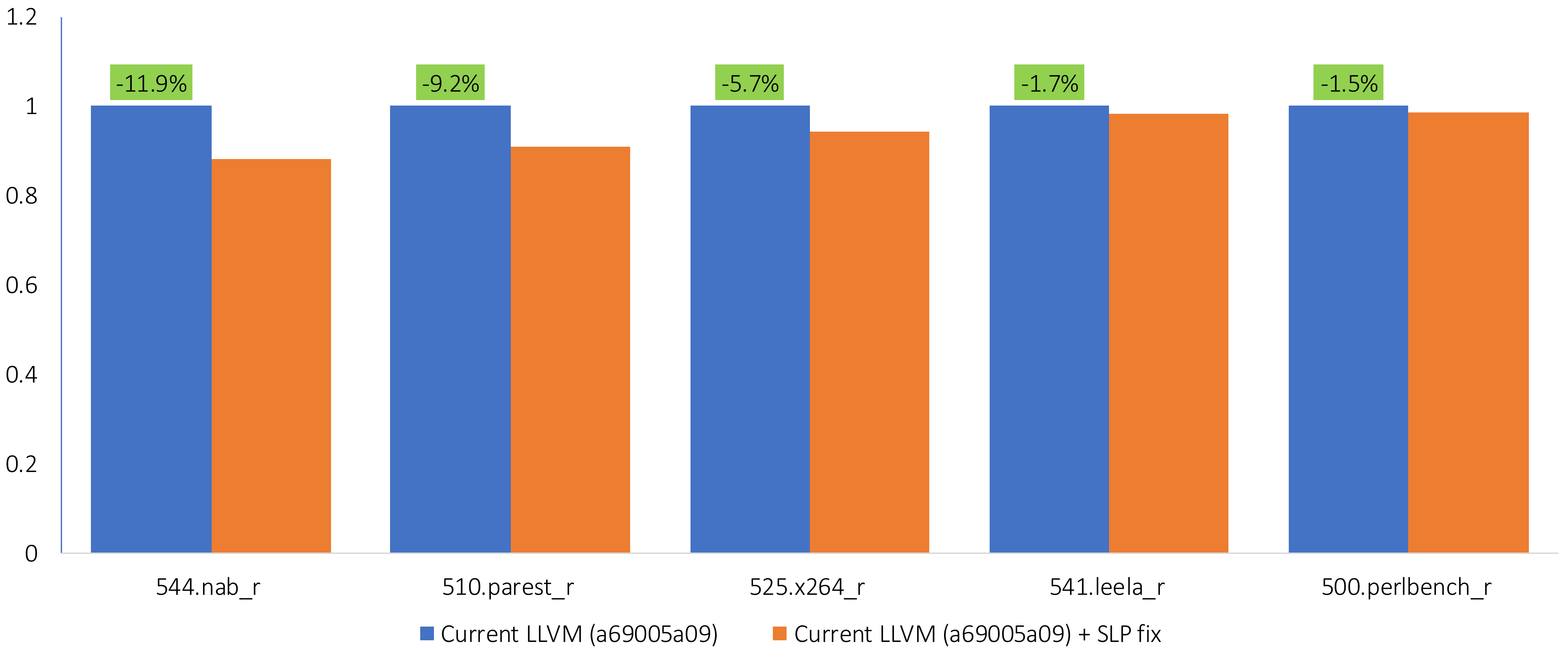
- But with a major drawback: **+6.9%** increase compilation time in 502.gcc_r.

Addressing the Issue

- To address the issue, we first proposed a patch which modified the SLP vectorizer to properly walk through all basic blocks when analyzing cost.
- Promising results: execution time dropped by **9.92%** in 544.nab_r.
- But with a major drawback: **+6.9%** increase compilation time in 502.gcc_r.
- Following discussions with the community, Alexey Bataev (SLP Vectorizer code owner) proposed and landed refined solution.

RVA22U64_V SPEC exec time, O3+LTO, SLP fix



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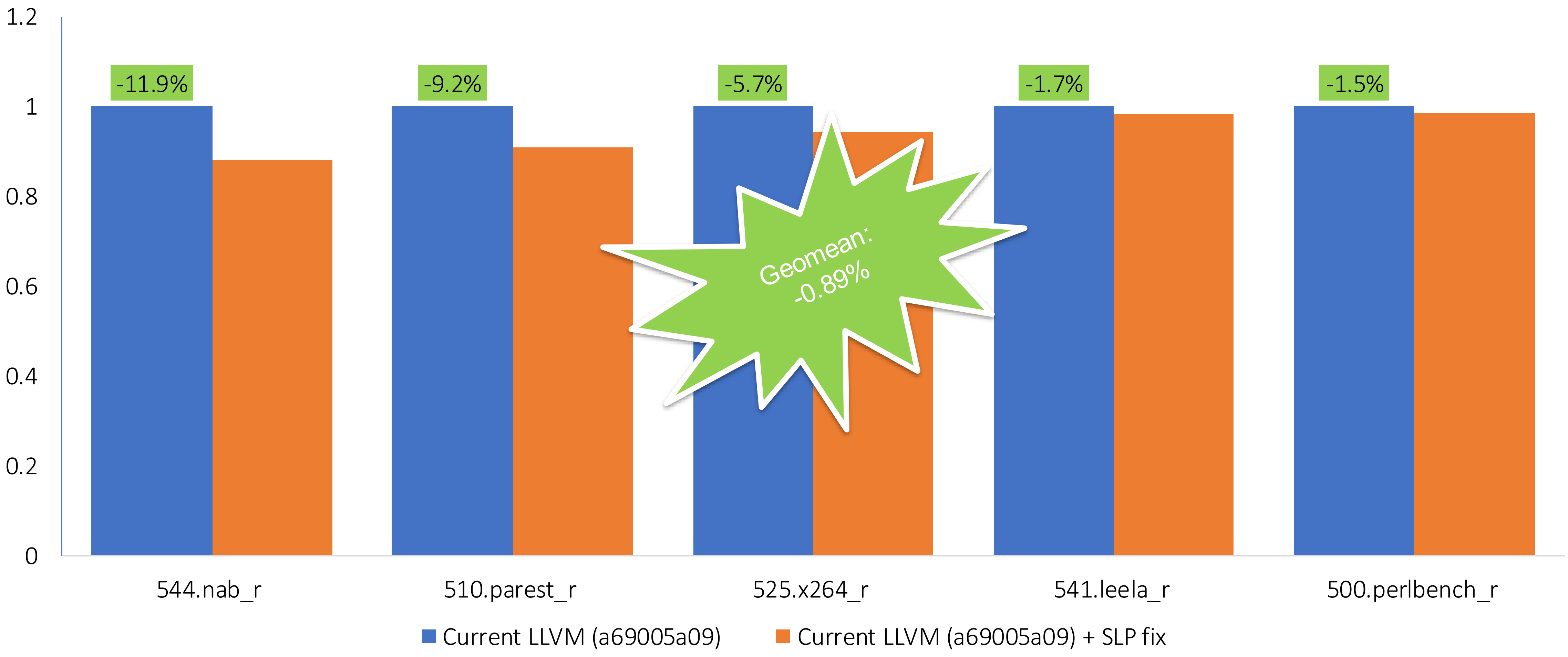

IPRA (Inter-Procedural Register Allocation) Support

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- IPRA: caller/callee register use is tracked across the functions, by eliminating unnecessary save/restore sequences.

What IPRA Brings

```
foo:
        addi    sp, sp, -32
        sd      ra, 24(sp)
        sd      s0, 16(sp)
        sd      s1, 8(sp)
        ...
        ld      s1, 8(sp)
        ld      s0, 16(sp)
        ld      ra, 24(sp)
        addi    sp, sp, 32
        ret
```

before

```
foo:
        addi    sp, sp, -8
        sd      ra, 0(sp)
        ...
        ld      ra, 0(sp)
        addi    sp, sp, 8
        ret
```

after

What IPRA Brings


```
foo:
      addi    sp, sp, -3
      sd      ra, 24(sp)
      sd      s0, 16(sp)
      sd      s1, 8(sp)
      ...
      ld      s1, 8(sp)
      ld      s0, 16(sp)
      ld      ra, 24(sp)
      addi    sp, sp, 32
      ret
```

saved even if not really live

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before

```
foo:
      addi    sp, sp, -8
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      ...
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      ret
```

after

What IPRA Brings

```
foo:
        addi    sp, sp, -32
        sd      ra, 24(sp)
        sd      s0, 16(sp)
        sd      s1, 8(sp)
        ...
        ld      s1, 8(sp)
        ld      s0, 16(sp)
        ld      ra, 24(sp)
        addi    sp, sp, 32
        ret
```

before

```
foo:
        addi    sp, sp, -8
        sd      ra, 0(sp)
        ...
        ld      ra, 0(sp)
        addi    sp, sp, 8
        ret
```

only what's truly needed

after

Impact of IPRA

- Reduction in register pressure, shorter prologue/epilogue code.

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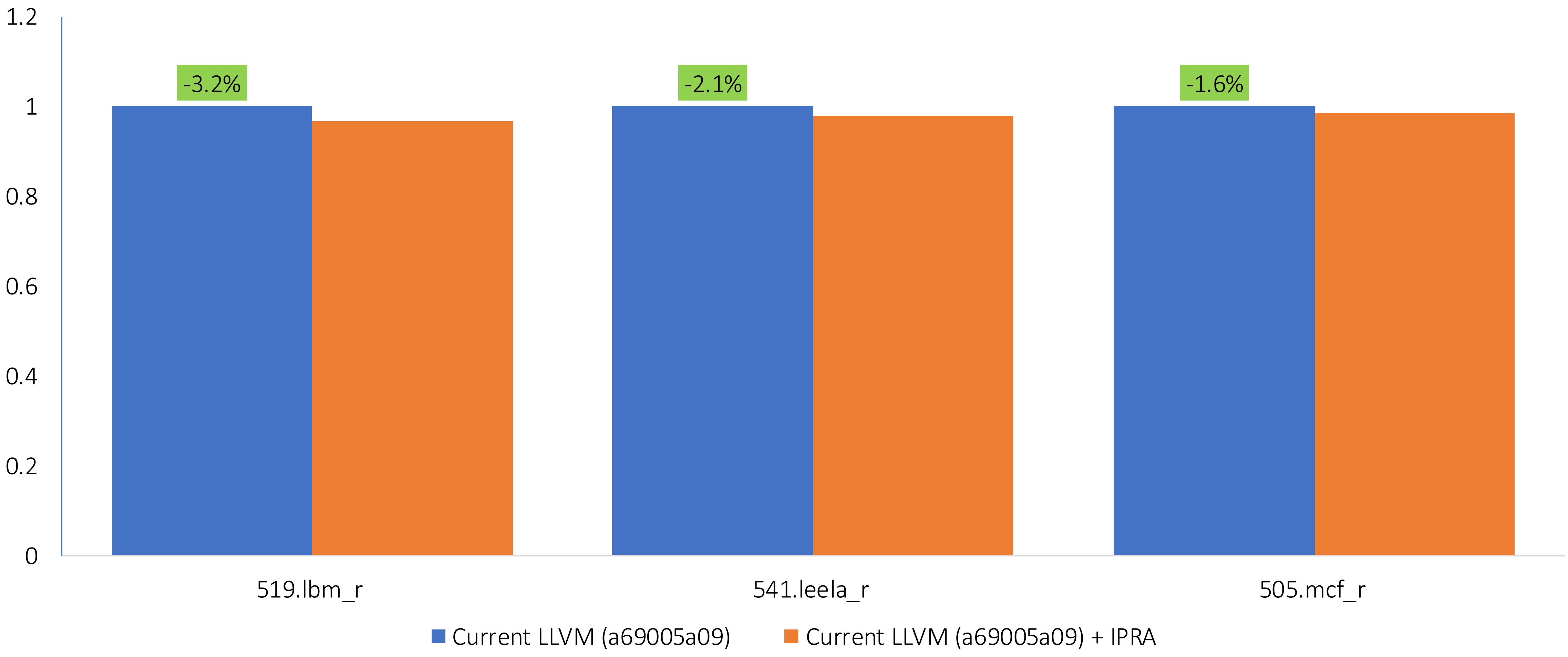
- SPEC benchmarks showed measurable improvements (small but consistent).

Impact of IPRA

- Reduction in register pressure, shorter prologue/epilogue code.
- SPEC benchmarks showed measurable improvements (small but consistent).
- Unfortunately, it can’t be enabled by default: IPRA is not enabled by default due to a bug (described in issue 119556), however, it does not affect the SPEC benchmarks.

RVA22U64 SPEC exec time, O3+LTO+IPRA



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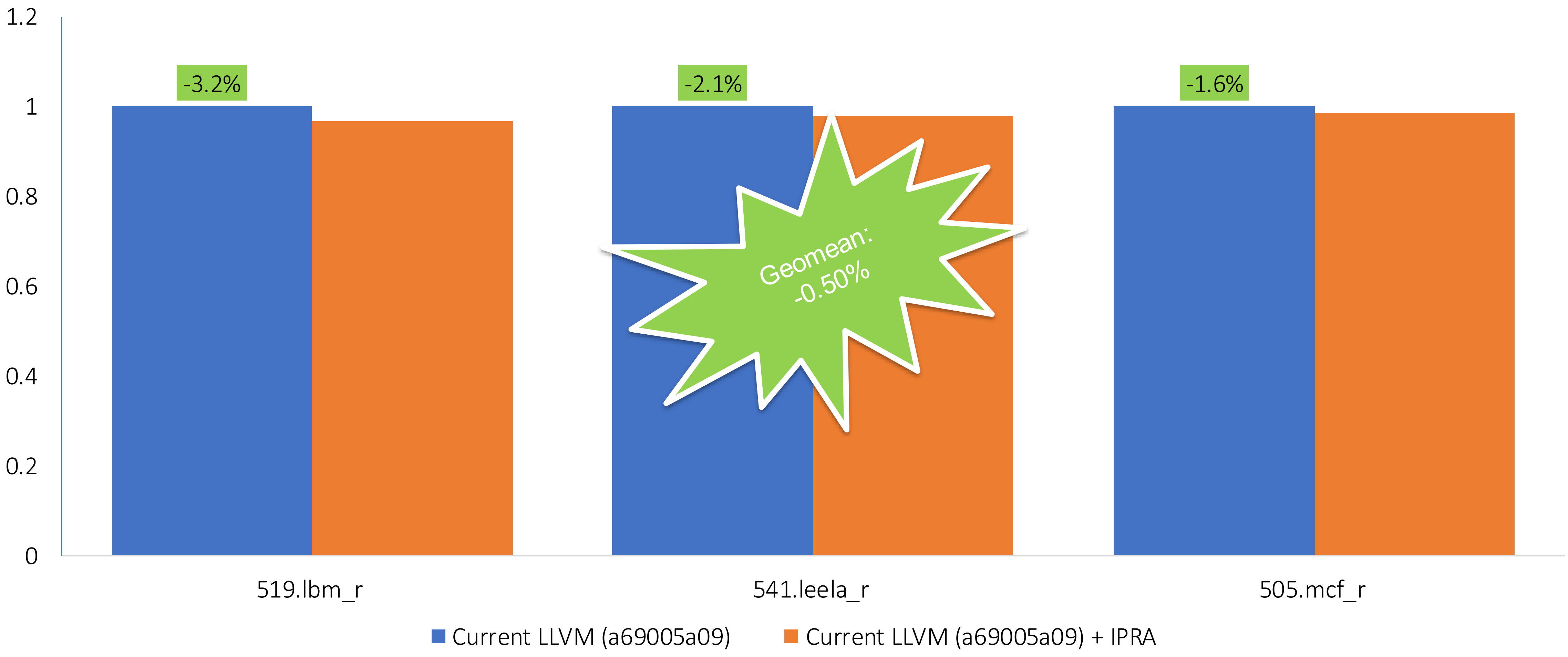
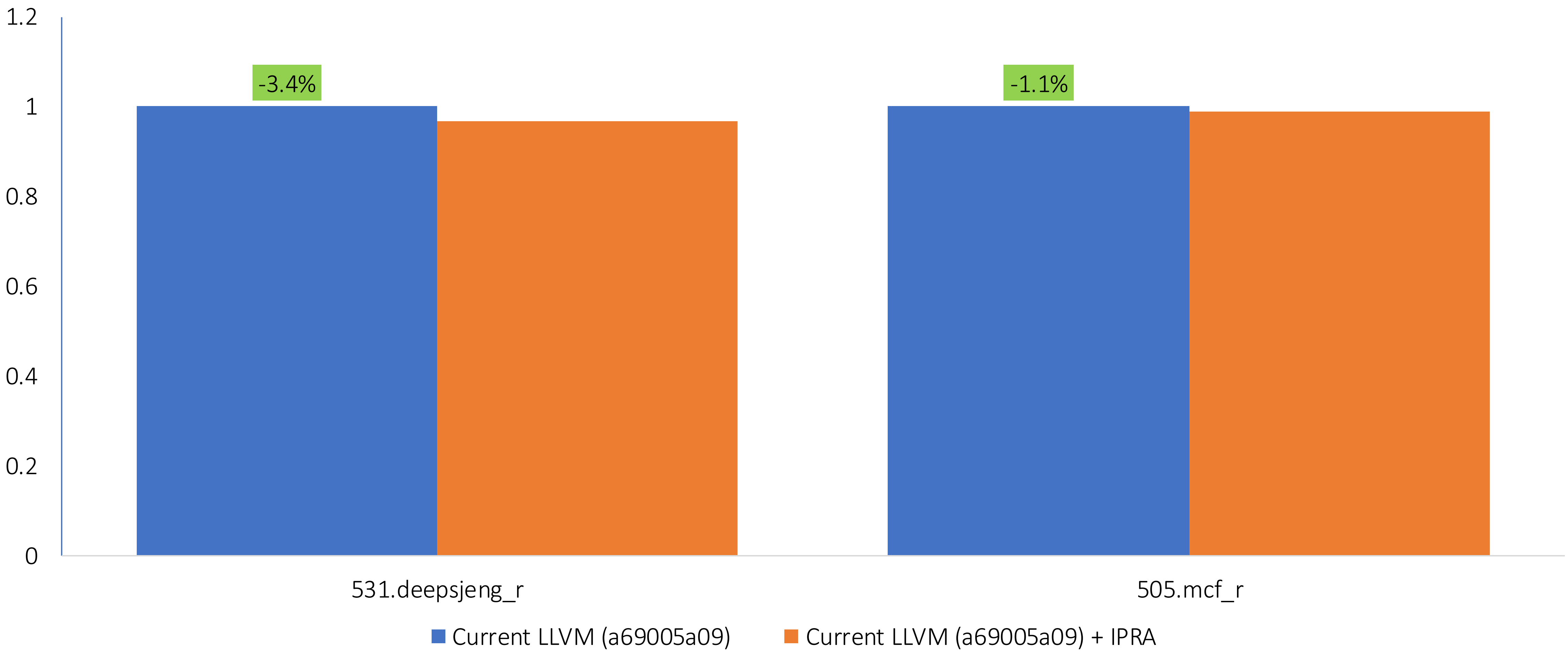


RVA22U64_V SPEC exec time, O3+LTO+IPRA



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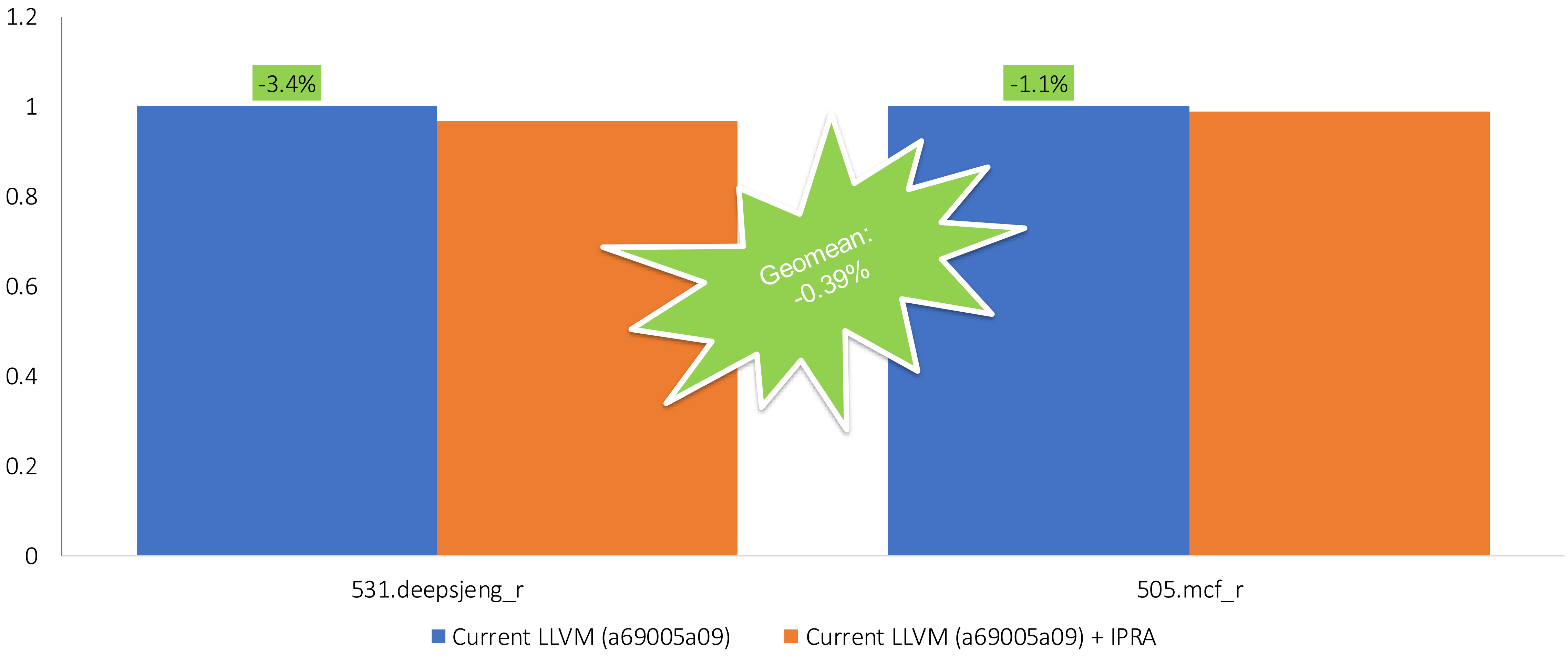

Conclusions

Faster RISC-V Today

- We contributed with:
  - Scheduling: largest wins, especially for scalar-heavy code.
  - Vectorization: enabled smarter spilling cost calculations.
  - IPRA: smaller but consistent improvements across workloads.

Faster RISC-V Today

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- We contributed with:
  - Scheduling: largest wins, especially for scalar-heavy code.
  - Vectorization: enabled smarter spilling cost calculations.
  - IPRA: smaller but consistent improvements across workloads.
- Almost all changes are upstream benefiting everyone. Under review:
  - https://github.com/llvm/llvm-project/pull/150618
  - https://github.com/llvm/llvm-project/pull/150644
  - https://github.com/llvm/llvm-project/pull/152557
  - https://github.com/llvm/llvm-project/pull/152737
  - https://github.com/llvm/llvm-project/pull/152738

What We Learned Along the Way

- Scheduling is critical for performance.
  - No scheduling model → LLVM pessimises the final code.
  - We should likely adopt some scheduling model as default, like other targets do.
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- Many contributions don't have immediate benchmark impact.
- Vectorization needs careful tuning to avoid regressions.

Did we close the performance gap between LLVM and the GCC compiler?

LLVM vs GCC on SpacemiT-X60

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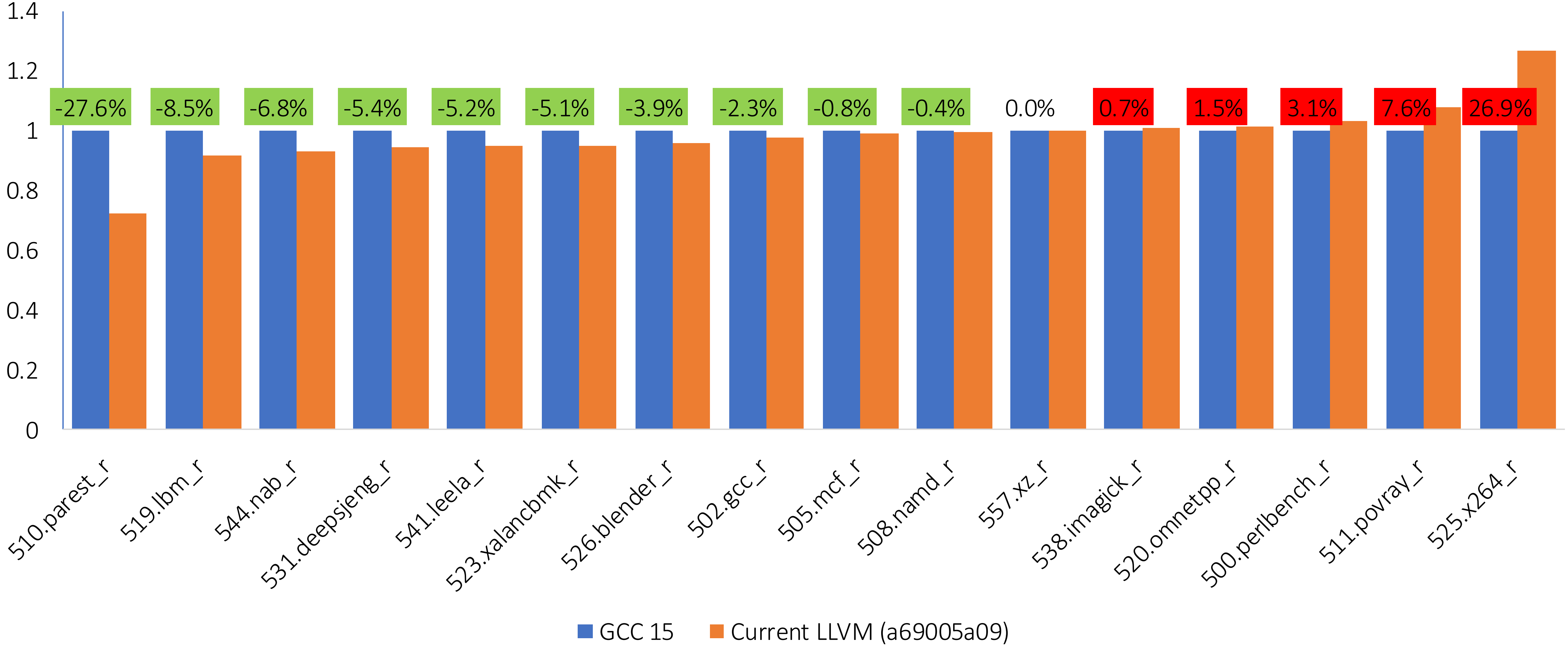
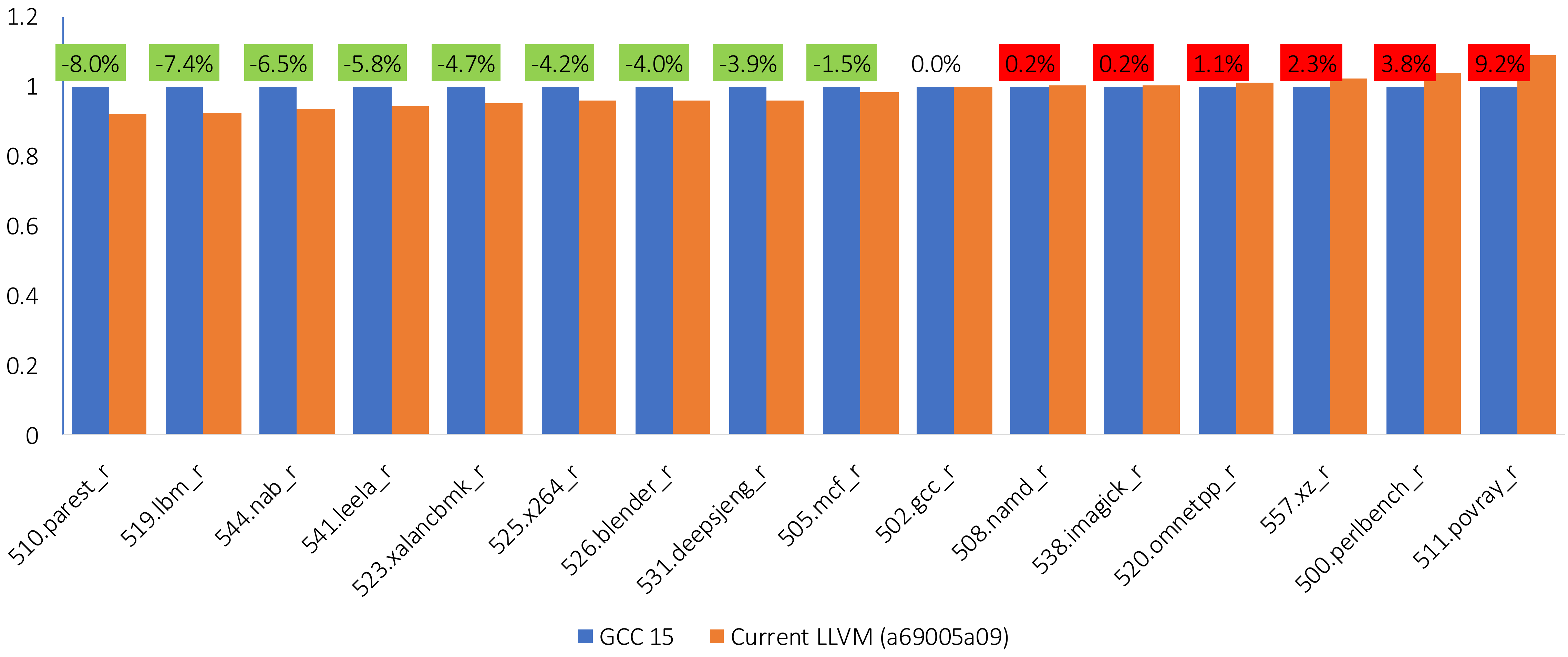
- But GCC doesn’t have X60-specific scheduling latencies, while LLVM does.
- Still useful to show relative progress and identify where LLVM has caught up.

RVA22U64 SPEC execution time, GCC vs LLVM



RVA22U64_V SPEC execution time, GCC vs LLVM



Thanks!

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- Thanks to my Igalia colleagues for discussions, and feedback.
- And to the LLVM RISC-V community for reviews and for getting patches upstream quickly.

RISC-V @ Igalia

- Accidental Dataflow Analysis: Extending the RISC-V VL Optimizer @ 2025 EuroLLVM by Luke Lau: https://www.youtube.com/watch?v=bkOwPr36SrQ
- Improvements to RISC-V Vector code generation in LLVM @ 2025 RISC-V Summit Europe by Luke Lau and Alex Bradbury: https://www.youtube.com/watch?v=0NjugW7FF48
- RISC-V nightly performance testing of top-of-tree GCC and clang:

  https://cc-perf.igalia.com/

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